PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of **Crockett**, et al : Date: December 13, 2002

Serial Number: 09/775,250 : Group Art Unit: 2841

Filed: February 01, 2001 : Examiner: I. Patel.

Title: **Insertion of Electrical Component within a Via of a Printed Circuit Board**

: IBM CORPORATION
Intellectual Property Law
Department 9CCA/Building 002/2
P.O. Box 12195
Research Triangle Park, NC 27709
: **Customer No. 25299**

REPLY AND AMENDMENT UNDER 37 C.F.R. § 1.111

Assistant Commissioner for Patents
Washington, D. C. 20231

Dear Sir:

This Amendment is submitted in response to the Examiner's Action dated August 14, 2002. Please amend the above-identified application as follows:

CERTIFICATE OF MAILING PURSUANT TO 37 C.F.R. §1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail under 37 C.F.R. §1.8 in an envelope addressed to the Assistant Commissioner for Patents and Trademarks, Washington D.C. 20231, on this day, the December 13, 2002.

Michele Fitzsimmons BY: MICHELE FITZSIMMONS

Signature

RPS920000103US1

In the Claims:

Please amend Claims 1 , 7, 10, and 19 as follows (Clean Version of Amended Claims):

1. A printed circuit board, comprising:
a plurality of conductive layers, wherein one of said plurality of conductive layers is a first layer, wherein one of said plurality of conductive layers is a second layer;
two or more vias interconnecting two or more conductive layers of said plurality of conductive layers, wherein a first of said two or more vias is part of a signal path configured to carry a signal from said first layer to said second layer, wherein a second of said two or more vias is part of a reference path configured to carry said signal from a third layer to a fourth conductive layer, wherein said fourth conductive layer returning said signal to a source; and
an electrical component embedded in said second of said two or more vias between two conductive layers of said plurality of conductive layers, wherein said electrical component has a greater diameter in a center than at ends of said electrical component, wherein each end of said electrical component has a tinned cap to promote solder residue adhesion to each end of said electrical component.

7. Canceled.

10. A printed circuit board, comprising:
a plurality of conductive layers;
two or more vias interconnecting two or more conductive layers of said plurality of conductive layers; and
an electrical component embedded in a particular via between two conductive layers of said plurality of conductive layers, wherein said electrical component has a greater diameter in a center than at ends of said electrical component, and each end of said electrical component has a tinned cap to promote solder residue adhesion to each end of said electrical component.

19. Canceled.

PRELIMINARY REMARKS

The present application sets forth Claims 1-7 and 9-19. Examiner has rejected all claims under 35 U.S.C. § 103(a) as being unpatentable over Kwong (6,388,890) in view of Takagi (4,800,459).

APPLICANT'S REPLY AND AMENDMENT

Consistent with the holding of Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co., Ltd., et al., 535 U.S. ___ (2002), decided May 28, 2002, any of Applicant's Replies and Amendments that hereafter are deemed to be narrowing amendments by a court of competent jurisdiction in a final unappealed or unappealable decision, are not intended to relinquish any scope of equivalents unforeseeable at the time of this amendment or that relate to aspects of the invention having only a peripheral relation to the basis for the amendment.

APPLICANT'S REMARKS

Applicant has amended certain claims of the instant application and believes that all remaining claims, amended and otherwise, now stand ready for allowance. On review of Examiner's comments, Applicant firstly believes that Examiner's cited §103(a) rejections are applied to the present invention based upon hindsight and are devoid of support for suppositions set forth by Examiner; however, in furtherance of prosecution of the Application on the merits, Applicant has amended the certain claims thereby responding to each of Examiner's assertions, and, in combination with the arguments following, provided the basis for rendering all §103 rejections moot. In view of such, Applicant respectfully requests removal of all rejections and objections, reconsideration all claims, and a timely notice of allowance to optimize Applicant's statutory patent term.

More particularly, Examiner has asserted that although either of Examiner's references refer, suggest, motivate or teach towards the tinning aspect as claimed by the present invention, that such would have been known by one of ordinary skill in the art (see Office

Action p5). Examiner states that "tinning is known in the art for better electrical connection" (see Office Action p5).

Applicant asserts that such a statement, while may holding true in other applications, is not the substantive basis for requiring tinning in the present invention. Of note, is that the use of tinning in the present application is not routine, but rather is an inventive and novel solution.

For the present invention, Applicant directs Examiner to page 12 of the instant Specification. As is evident, the present invention details that although each end of electrical component may have a conductive cap that is tinned, i.e., covering conductive cap with a tin alloy, that by having each end of electrical component tinned, solder residue sticks to the end of electrical component that is tinned. Since the central diameter of electrical component is greater than the outer ends of electrical component, solder residue may be prevented from flowing around the center of electrical component thereby preventing the shorting of electrical component. Furthermore, side view of printed circuit board illustrates via interconnected to layer 210B and layer 210E as illustrated by the thick lines intersecting via 250B at layers 210B and 210E. It is noted that via 250B may be interconnected between any two separate conductive layers 210, e.g., layers 210A-F.

Applicant notes that disclosed use of tinning for the present invention is not as proposed by Examiner - on the contrary, tinning is used to prevent short circuiting and not to improve electrical conductivity.

Additionally, Applicant notes that the practice of adding additional surfaces (i.e., tinning) in this field is in practice antithetic to the objectives of minimizing the number of features within. As becomes obvious, tinning only adds to the complexity and if such were indeed an ordinary solution would such not already have been "routinely" implemented?

Applicant believes Examiner's references and reasoning do not include teachings, motivations or suggestions evidencing Examiner's supposition, fail to account for the

inventive efforts and novelty set forth in the present application, fail to recognize that the present invention is substantively different from said references, and fail to account for Applicant's use of tinning contradistinctively from that "believed' by Examiner.

Contradistinctively, Applicant has claimed the present invention based upon quite non-routine efforts and novel approaches.

Further, Applicant believes that the Examiner has, in error, cited the present invention as being obvious as a direct result of and in clear view of the present application. The present application discloses features and/or functions of the invention which had not heretofore been considered in the cited prior art, and which would not have been asserted as obvious upon examination *but for* the disclosure itself. Applicant asserts that such hindsight reasoning is clearly an improper basis for the finding of obviousness[1] as the cited prior references do not teach, disclose or suggest that which is disclosed in the present application.

In particular, there is no teaching or suggestion in any of Examiner's references, nor in that of the cited references, as to why the skilled artisan would use the specific augmentation as set forth by the Examiner. Further, for purposes of appeal, the Courts

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[1] See, e.g., In re Gorman, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Federal Circuit 1991) ("As in all determinations under 35 U.S.C. §103, the decision maker must bring judgment to bear. It is permissible to, however, simply to engage in a hindsight reconstruction of the claimed invention, using applicant's structure as a template and selecting elements from references to fill the gaps."); Symbol Technologies Inc. v. Opticon Inc., 17 USPQ2d 1737, 1746 (S.D.N.Y. 1990) aff'd, 935 F.2d 1569, 19 USPQ2d 1241 (Fed. Cir. 1991) ("That a technician, in hindsight, could combine elements known within the technology to produce the contested patent does not make the patent obvious to one skilled in the art at the time the patent was issued."); In re Dow Chemical Co., 837 F.2d 469, 473, 5 USPQ2d 1529, 1531 (Fed. Cir. 1988) ("The consistent criterion for determination of obviousness is whether the prior art would have suggested to one of ordinary skill in the art that this process should be carried out and would have a reasonable likelihood of success, view in light of the prior art...Both the suggestion and the expectation of success must be founded in the prior art, not in the applicant's disclosure."); Medtronic, Inc. v. Cardiac Pacemakers, Inc., 721 F.2d 1563, 1582 (Fed. Cir. 1983) ("whether the references, taken as a whole, would suggest the invention to one of ordinary skill in the art);

have held that "[w]ith respect to core factual findings in a determination of patentability, the Board cannot simply reach conclusions based on its own understanding or experience – or on its assessment of what would be basic knowledge or common sense."[2]

Therefore, Applicant is not accepting of the attempt by Examiner to simply reject without any evidence to support the basis or assertion as motivation for modifying the references. As the underlying cited art, individually or in combination with Examiner's other cited references, neither discloses each and every claim limitation, nor suggests or teaches towards the present invention, Applicant believes the Examiner has failed to establish a *prima facie* case of obviousness. Accordingly, Applicant believes that as the prima facie case has failed, the references, individually or in combination do not support a position of affirming the Examiner's rejections, whether a reliance is placed on one or all of the cited art.[3]

Similarly, for all of the reasons above, the cited art, alone or in combination, does not render obvious nor anticipate Applicant's invention.

ALL REMAINING CLAIMS STAND READY FOR ALLOWANCE

Applicant has amended claims 1, 7, 10, and 19 to more precisely claim Applicant's invention and clarify the invention. In particular, Applicant has amended independent claims 1 and 10 to include variants of tinning limitation terms of depending claims 7 and 19, respectively, along with additional terms indicative of promotion of solder residue adhesion (found in the Specification, p 12), and has canceled claims 7 and 19. Applicant asserts said amended Claims now stand ready for allowance as all §103 rejections, for all of the reasons above, are rendered moot. Accordingly all dependent claims depending variously therefrom also stand ready for allowance.

REQUEST TO PROCEED TO ALLOWANCE

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[2] *In re Zurko*, No. 96-1258 (Fed. Cir. August 2, 2001).

[3] *See In re Bush*, 296 F.2d 491, 496, 131 USPQ 263, 266-67 (CCPA 1961).

For each and all of the reasoning set forth above, and as Applicant believes each and all of Examiner's objections and rejections have been traversed, Applicant requests that the application be reconsidered and a timely notice of allowance be issued.

COMPLIANCE PER 37 C.F.R. § 1.121 and § 1.125

Applicant has included Attachment "A" hereto, entitled"**Version with Markings to Show Changes Made**", which is demonstrative that no new matter has been introduced, and which details changes made to the Specification and Claims, by the present Amendment.

ADMINISTRATIVE MATTERS

Applicant requests that Examiner ensure future correspondence be directed to the Attorney undersigned hereto, and that the record be updated to reflect the undersigned as the **Attorney of Record** for all matters henceforth. The Examiner is invited to contact the undersigned for any and all matters related to this Application.

Respectfully submitted,

By _____

J. BRUCE SCHELKOPF
Registration No.: 43,901
Attorney for Applicants
IBM CORPORATION
Department 9CCA/Bldg. 002-2
P.O.Box 12195
Research Triangle Park, NC 27709
(919) 543-4753
schelkop@us.ibm.com